

# Influence of Parasitic Capacitances in Modeling and Analysis of Advanced Floating Gate Memory Devices

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**Abstract-** In this paper, we report the impact of the parasitic capacitances in the modeling and analysis of advanced floating gate (FG) non-volatile memory (NVM) devices, especially on the coupling ratio. Due to the poor accuracy of the existing capacitance model when compared to practice, an approach to include the parasitic capacitances has been established. Measurement results from two transistor (2T) Fowler-Nordheim (FN) tunneling operated flash memory show a good improvement in the model accuracy. The parasitic capacitances depend very much on the floating gate dimension, and the spacing to the neighboring elements in the flash cell array. The growing influence of the parasitic capacitances and the subsequent degradation of the existing model accuracy can be expected for the cells dimensions in future process technologies. With the accurate calculation method for the parasitic capacitances proposed in this paper, the cell characteristics can be more accurately modeled, and the degradation of the cell can be accurately studied.

## I. INTRODUCTION

The Non-Volatile memory (NVM) sector today occupies one of the largest portions of semiconductor market, with application areas like portable storage/data-transport, digital camera/video storage, and storage medium for media players. Technology-wise, it has become a driving force for semiconductor technology scaling. NVM devices have also been successfully implemented in embedded systems (like system on chip, SOC), for application areas like e-passports, smart-cards, and micro-controllers. These application areas with embedded NVM have very high requirements on reliability. A high reliability requires a good understanding and accurate modeling of the device right from the development phase.

This paper addresses accurate modeling of the capacitances and coupling ratio (basic but very important parameters) in floating-gate based NVM devices. We report that the parasitic capacitances are becoming more and more important in technology scaling, and that they can be easily modeled in an accurate way. Furthermore, since the floating gate size increasing is a technique widely used by engineers to increase cell coupling ratios, the influence of the floating gate dimensions in these capacitive parameters (for the same technology node) is also studied and reported.

The calculations are applied to a 2T-FNFN-NOR device from

a state-of-the-art technology [1], being verified with experimental data obtained from a large amount of memory cells, to avoid cell-to-cell variation effects. Fig. 1 shows the schematics and transmission electron microscopy (TEM) cross-section of such a 2T-FNFN-NOR device.

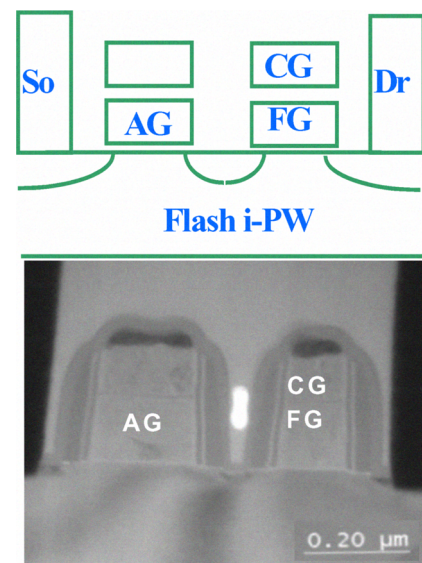


Fig. 1. Top: A schematic cross section of the two-transistor cell. Control gate (CG) and floating gate (FG) are on the right side near the drain (Dr) while the access gate (AG) is on the left side near the source (So). Bottom: TEM cross-section of the two-transistor cell in 90nm node.

## II. MODELS

Although a 2T-FNFN-NOR device has been used as a concrete example in our calculations, the method being proposed is applicable to other NVM floating gate devices.

Fig. 2 shows a 3-D drawing of the cell with channel, floating gate (FG) and access gate (AG). The control gate (CG) is not drawn to simplify the view.

### A. Simplified Capacitance Model

The 2T-FNFN-NOR uses uniform Fowler-Nordheim (FN) tunneling through the tunneling area to program and erase the cells. The current density through the tunnel oxide is governed by the FN equation:

$$J_{OX} = \alpha \cdot E_{OX}^2 \cdot (\exp(-\beta / E_{OX})) \quad (1)$$

where  $E_{OX}$  is the electric field across the oxide, and  $\alpha$  and  $\beta$  are tunneling constants.  $E_{OX}$  is given by:

$$E_{OX} = \frac{|V_{OX}|}{t_{OX}} \quad (2)$$

where  $V_{OX}$  is the voltage drop across the oxide and  $t_{OX}$  is its thickness. For a certain amount of charge stored in the FG,  $V_{OX}$  can be expressed for program and erase operations ( $|V_{OX}|_P$ ,  $|V_{OX}|_E$ ), as a function of the applied potential in the CG ( $V_{CG}$ ), in terms of a simple coupling ratio:

$$|V_{OX}|_E = K_{CG} \cdot (V_{CG} - V_t + V_m) + V_{fb} \quad (3)$$

$$|V_{OX}|_P = K_{CG} \cdot (V_{CG} - V_t + V_m) \quad (4)$$

where  $V_t$  is the threshold voltage of the cell,  $V_m$  is the threshold voltage when there is no charge stored in the FG,  $V_{fb}$  is the flat band voltage and  $K_{CG}$  is the coupling ratio that denotes the fraction of  $V_{CG}$  which will appear across the tunnel oxide.  $K_{CG}$  can be obtained from the various capacitances in the cell as:

$$K_{CG} = \frac{C_{IPD}}{C_{IPD} + C_{OX}} \quad (5)$$

where  $C_{IPD}$  is the inter-poly dielectric capacitance, i.e. the capacitance between FG and CG, and  $C_{OX}$  is the tunnel oxide capacitance, i.e. the capacitance between FG and the channel. These capacitances are approximately calculated using a parallel plate capacitor model and neglecting any fringe or parasitic capacitance, which leads to:

$$C = \frac{\epsilon \cdot \epsilon_0 \cdot A}{d} \quad (6)$$

where  $\epsilon$  is the dielectric permittivity,  $\epsilon_0$  is the empty space permittivity,  $A$  is the plates' area and  $d$  the distance between them.

### B. The modified model including parasitic capacitances

The approximation as described in equation (6) worked pretty well in old technologies (down to sub-micrometer node) [3], but became inaccurate since the technology entered the deep-sub-micrometer era, due to the existence of many non-negligible parasitic capacitances in the cell.

To estimate these parasitic capacitances we split the cell's geometry in small parts that can be approached by parallel, orthogonal, or in line configurations. Fig. 2, schematically shows such various fringe/parasitic capacitances in a typical 2T-FNFN-NOR memory cell with a classic bar form FG.

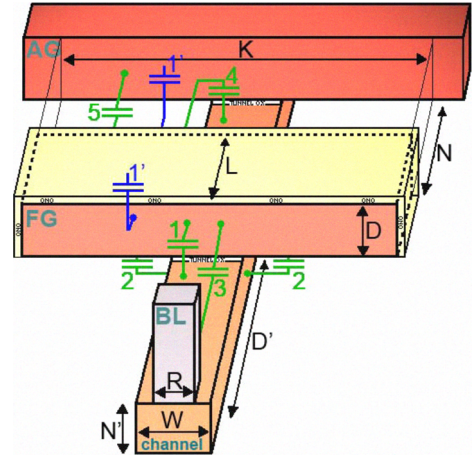


Fig. 2. Schematic geometry of a 2T-FNFN-NOR memory cell. The stacked CG above FG is omitted in the drawing. The bit line (BL) corresponds to the cell's drain. Cell's dimensions indicated in black and parasitic capacitances in green and blue. Capacitances labeled with the same number are symmetrical and have the same value.

Calculating fringe capacitances without using finite-element-methods (FEM) requires a correct formulation for the capacitance between non-parallel plates. Fig. 3 shows a schematic of a capacitor with two plates with the same area  $w \cdot l$ , oriented with angle  $\theta$  in the  $l'$  direction, and with a distance  $l_0$  from the origin (O) to the plate edge. Assuming that the electric field lines are semi-circular and considering (6) for an infinitesimal area section  $w \cdot dl'$ , the capacitance between the two plates can be obtained by solving the integral:

$$C \approx \int_{l_0}^{l_0+l} \frac{\epsilon \cdot \epsilon_0 \cdot w}{\theta \cdot l'} dl' \quad (7)$$

which leads to:

$$C \approx \frac{\epsilon \cdot \epsilon_0 \cdot w}{\theta} \ln \left( \frac{l + l_0}{l_0} \right) \quad (8)$$

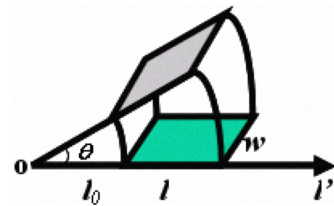


Fig. 3. Schematic of a capacitor with non-parallel plates in the  $l'$  direction. This model is used for the analytic calculation of the fringe capacitances.

Special attention needs to be paid to the permittivity of the different dielectric materials ( $\epsilon$ ) in the fringe/parasitic capacitors.

After considering the parasitic capacitances, the coupling ratio formula becomes:

$$K_{CG} = \frac{C_{IPD} + C_{fg-cg,p}}{C_{IPD} + C_{fg-cg,p} + C_{OX} + C_{fg-rest,p}} \quad (9)$$

where  $C_{fg-cg,p}$  is the total parasitic capacitance between FG and CG (represented by the blue capacitances in fig. 2), and  $C_{fg-rest,p}$  is the total parasitic capacitance from FG to all the rest nodes (represented by the green capacitances in fig. 2).

For a classic bar-form FG cell in the 45nm technology node, we have calculated the coupling ratio, as a function of the floating gate width ( $K$ ) and height ( $D$ ), fixing the channel area ( $W=60\text{nm}$ ,  $L=60\text{nm}$ ) and all the other cell's dimensions (see fig. 2). Fig. 4 shows the calculated results with (bottom graph) and without (top graph) taking the parasitic/fringe capacitances into account. As shown, for the various dimensions of the FG there is always a significant difference between the coupling ratios obtained with and without the parasitic/fringe capacitances.

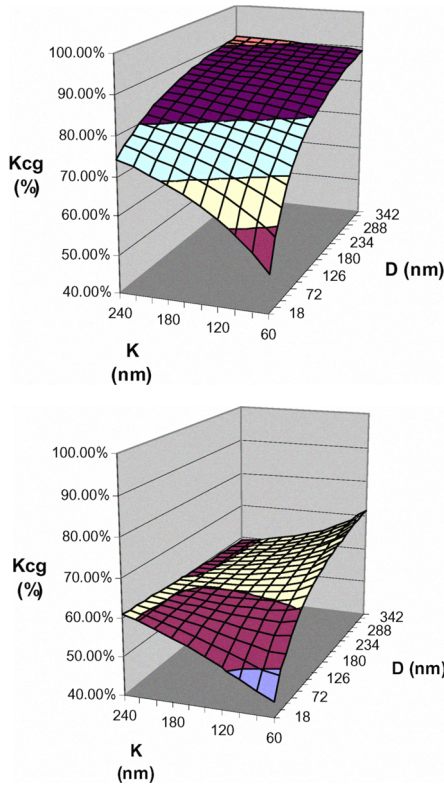


Fig. 4. Dependence of  $K_{CG}$  with the  $D$  and  $K$  dimensions of the FG. Top: traditional model. Bottom: model taking into account the parasitic capacitances.

From Fig. 4 one concludes that increasing the FG height and width will increase the coupling ratio, but only till a certain point, after which increasing these dimensions will cause almost no raise or even a drop on the coupling ratio. E.g. for a FG  $D$  above 100 nm, the increase of the FG  $K$ , has almost no effect on the coupling ratio, actually causing it to decrease specially when  $K$  is still close to the channel width. This happens due to a big raise of the parasitic capacitances 2 and 5 (see fig. 2) when we start raising  $K$ , which in the case of a high FG  $D$ , is not

compensated by the smaller increase of the parasitical capacitance 1' added to the normal increase of  $C_{IPD}$ .

Thus, the point where  $K_{CG}$  is maximum, is no longer for maximum  $K$  and  $D$  but actually for maximum  $D$  and minimum  $K$ .

Fig. 5 plots the relative error introduced by using the simplified capacitance model. It makes clear that the error is higher as both FG dimensions increase, which means a much smaller  $K_{CG}$  value than expected from the simple model.

Since increasing the FG dimensions is a common practice to increase  $K_{CG}$ , the previous result shows that special attention should be paid to the parasitic capacitances when performing this operation, in order to obtain an actually higher  $K_{CG}$ .

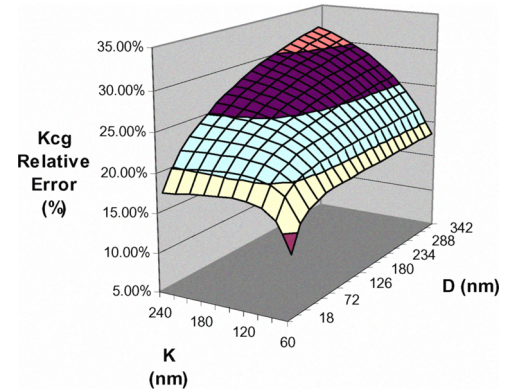


Fig. 5. Relative error introduced in  $K_{CG}$  calculation by neglecting the parasitic capacitances.

### III. EXPERIMENTAL VALIDATION

Measurements have been carried out on 2.7Mbit arrays of devices fabricated in 90nm embedded NVM technology during development phase, and the median results for the array population were considered in order to avoid cell-to-cell variation effects.

First, gate current density measurements ( $J_G-V_G$ ) were performed on a FG directly connected array. These measurements prove that the measured gate current is governed by the FN equation, with values for  $\alpha$  and  $\beta$  in accordance to the ones reported by Kolodny [5]. Fig. 6 shows the measured  $J_G-V_G$  curve and the best-obtained fit with the FN equation.

In a FG cell (FG really floating), the tunneling current can be extracted from program/erase speed measurements, i.e. the threshold voltage change in time [1-3], if  $K_{CG}$  and  $C_{IPD}$  are known.

As shown in the graph of fig. 7, a large error exists (between the calculated and measured  $J_G-V_G$  curves) if  $K_{CG}$  and  $C_{IPD}$  are calculated without including the parasitic capacitances. In contrast, when taking into account the parasitic capacitances to determine  $K_{CG}$ , an excellent agreement can be obtained.



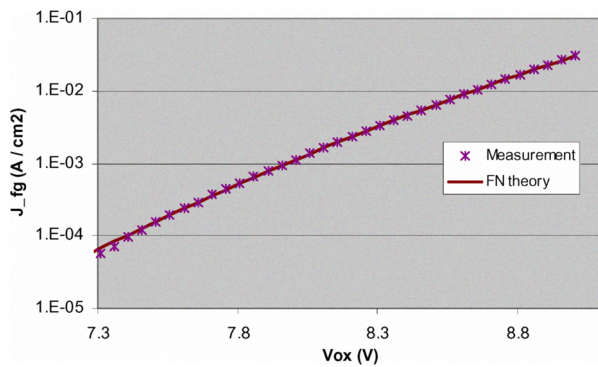


Fig. 6. Gate current density measured with the potential directly applied to the FG. Fitting with the FN equation obtained with  $\alpha=1.23\text{E-}05 \text{ A/V}^2$  and  $\beta=2.60\text{E+}10 \text{ V/m}$ , and considering  $V_{fb}=0.992 \text{ V}$ .

The data shown in fig. 7 were obtained from an un-stressed (thus fresh) cell with a classic bar form FG, considering for the FN approximation the  $\alpha$  and  $\beta$  values obtained from the  $J_G$ - $V_G$  measurement and a standard  $V_m$  for an uncycled cell of  $0.806 \text{ V}$ .

When considering a stressed cell with 100K program/erase cycles, the fit is still very accurate as shown in fig. 8. This fit for the cycled cell was obtained with  $V_m=1.46\text{V}$ , which shows a  $V_m$  degradation of  $0.654 \text{ V}$  compared to the fresh cell.

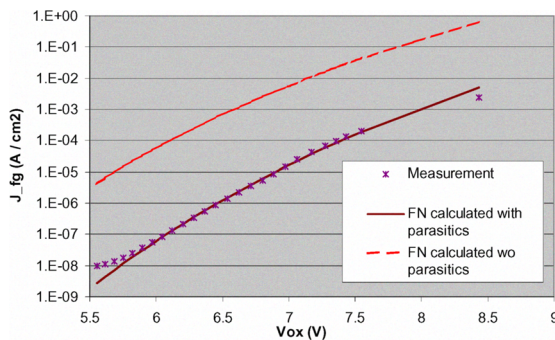


Fig. 7. Measured gate current density and respective fit with the FN equation for fresh cells. FN approximation obtained with and without considering the parasitic capacitances and  $V_m=0.806 \text{ V}$ .

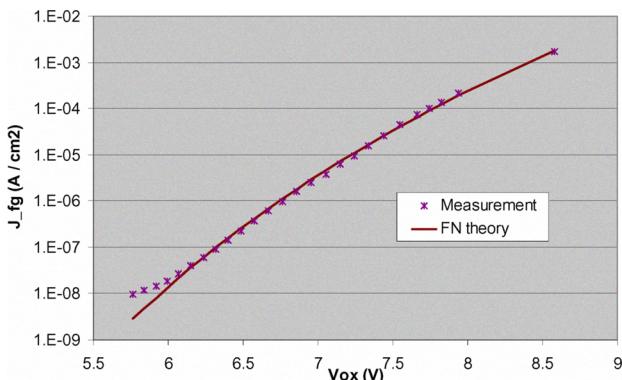


Fig. 8. Measured gate current density and respective fit with the FN equation for cells stressed with 100K program/erase cycles. FN approximation obtained taking into account the parasitic capacitances and considering  $V_m=1.46 \text{ V}$ ,  $\alpha=2.5\text{E-}06 \text{ A/V}^2$ , and  $\beta=2.59\text{E+}10 \text{ V/m}$ .

For this cell, the traditional capacitance model predicts  $K_{CG}=83.9\%$ , while the model including the parasitic capacitances predicts  $K_{CG}=71.4\%$ . Note that the gate currents in fig. 6, fig.7 and fig. 8 were extracted from measurements on cell structures from the same wafer to avoid issues caused by process variations.

#### IV. DISCUSSIONS

As described above, for the 90nm technology node cell used in our measurements,  $K_{CG}$  can be simply about  $14.9\%$  (relative error) lower than expected when the parasitic capacitances are neglected. When moving the same cell for a 45nm technology, the traditional model predicts  $K_{CG}=89.1\%$ , an absolute increase of  $5.2\%$  (due to a strong reduction of the capacitance  $C_{ox}$ ) compared to the 90nm technology. However, when looking to the model including the parasitic capacitances,  $K_{CG}=67.4\%$  is obtained, actually leading to an absolute  $K_{CG}$  decrease of  $4\%$  when compared to the 90nm technology. Thus, the relative error introduced in the  $K_{CG}$  calculation by using the simplified capacitor model in a 45nm technology, will increase to  $24.3\%$  and it will keep increasing as we downscale the technology.

Fig.9 shows the evolution of  $K_{CG}$  for the same kind of cell used in our measurements, built in different technology nodes (downscaling the horizontal dimensions). As we can see, the error is higher for smaller technologies, besides it is clear that when considering the parasitic capacitances for technologies below  $180\text{nm}$ ,  $K_{CG}$  will actually decrease as we downscale the cell, in opposition to the prediction obtained neglecting these parasitic capacitances.

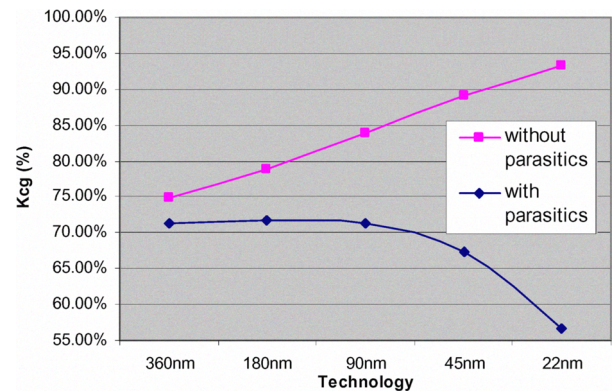


Fig. 9.  $K_{CG}$  evolution with technology downscaling. Values obtained for the same cell used in our measurements, downscaling all the horizontal dimensions.

In addition, the parasitic capacitances can affect the performance of the cell, lowering the coupling ratio and causing extra stress in some of the cell's components, as coupling ratios above  $70\%$  are very important to keep the program/erase potentials in a low value, to avoid damage on the oxide-nitride-oxide (ONO) layer and to maximize the cell's window. Therefore, these parasitic capacitances need to be minimized in future technologies.

Note also, that the coupling ratio and the tunneling constants  $\alpha$  and  $\beta$ , are not symmetric for program and for erase operations. In this paper, the  $K_{CG}$  values as well as the  $J_G$ - $V_G$  curves, are obtained for the erase operation. Nevertheless, during the execution of this work, the same process has been applied to the program operation and the results are in close agreement with the ones being published here.

## V. CONCLUSIONS

When the parasitic capacitances are neglected, the simple model proposed by Kolodny [5] can no more describe the floating-gate cell characteristics in deep-sub-micrometer technologies, although the physics stays the same. Extending the usage of the Kolodny model requires an accurate calculation of the coupling ratio by including the parasitic capacitances  $C_{fg-cg,p}$  and  $C_{fg-rest,p}$  in the cell. This paper shows how these parasitic capacitances can affect the  $K_{CG}$  calculations.

We conclude that for an 180nm technology node, the parasitic capacitances already cause a significant  $K_{CG}$  lowering, which becomes stronger for the current small dimension technologies. It is also shown that, the importance of these parasitic capacitances increase even more as we try to increase  $K_{CG}$  by increasing the FG size. It is therefore imperative to include them in the  $K_{CG}$  calculations for current and especially for future technologies.

With the accurate calculation method for the parasitic capacitances proposed in this paper, the cell characteristics can be more accurately modeled, and the degradation of the cell can be accurately studied.

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